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| 10/680,126 | 10/08/2003 | Brian K. Langendorf | NVID-067/00US | 4684 |

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| EXAMINER | |
|---|---|
| KRAVETS, LEONID | |
| **ART UNIT** | **PAPER NUMBER** |
| 2189 | |

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|---|---|---|---|
| ***Office Action Summary*** | **Application No.**<br>10/680,126 | **Applicant(s)**<br>LANGENDORF ET AL. | |
| | **Examiner**<br>Leonid Kravets | **Art Unit**<br>2189 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Durrant (US PG Pub 2003/0028746).

4. As per claim 1, Durrant discloses in a memory system, a method for maintaining multiple copies of data, the method comprising

detecting a write by a first processor to a memory associated with a second processor (Paragraph 18);

determining whether the write to said memory is directed to a memory space to be shadowed [(Durrant describes data can be one of four states (Paragraph 15, Paragraphs 86-90)]; and

when the write to said memory is detected to a memory space to be shadowed, cloning the write and storing the cloned write in a second memory (Paragraph 15).

5. As per claim 2, Durrant discloses the method of claim 1 wherein said memory is a local memory and said second memory is a main memory [Durant discloses general first memories, first memory is interpreted as local memory, second memory interpreted as main memory (Paragraph 13)].

6. As per claim 3, Durrant discloses the method of claim 1 wherein said storing comprises translating an address of the shadowed region of the local memory to an address in the system memory (Paragraph 11 and 14).

7. As per claim 4, Durrant discloses a method for enhancing memory access in a multiple processing unit system including a central processing unit, a second processor,

a local memory associated with the second processor and a system memory, the method comprising:

associating a shadow mask bit and a region of the local memory [Since each WO bit is assigned to write data, the WO bit is associated with a region of the local memory the data is written into (Paragraph 86-90)];

identifying the region of the local memory as a region for shadowing by placing the associated shadow mask bit in a first state (Paragraph 86-90);

detecting a write operation to the region of local memory by the central processing unit (Paragraph 18);

detecting that the shadow mask bit associated with the region is in said first state [Memory management unit must check state of WO bits, to decide where to translate the data];

cloning the write operation [When WO is 11, write operation is cloned to both memories (Paragraph 90)]; and

writing the cloned write operation to system memory (Paragraph 18).

8. As per claim 5, Durrant discloses the method of claim 4 wherein the writing the cloned write operation comprises translating an address of the first region in local memory to an address in system memory (Paragraph 15); and

storing data from the write operation to the address resulting from the translating operation (Paragraph 15).

9. As per claim 6, Durrant discloses the method of claim 4 further comprising:

associating a second region of the local memory with a second shadow mask bit [Since each WO bit is assigned to write data, the WO bit is associated with a region of the local memory the data is written into (Paragraph 86-90)];

identifying the second region of the local memory as a region that is not to be shadowed by placing the associated second shadow mask bit in a second state (Paragraph 88);

detecting a write operation to the second region of local memory by the central processing unit [All write operations are detected by the memory management unit (Paragraph 11)];

detecting that the second shadow mask bit is in the second state [Memory management unit must check state of WO bits, to decide where to translate the data]; and

processing the write operation to the local memory without creating a shadow copy of the write operation in the system memory [Since WO bit says write to primary, data would only be written to the local memory without creating a shadow copy (Paragraph 88)].

10. As per claim 7, Durrant discloses the method of claim 6 further comprising:

resetting the second shadow mask bit to the first state [New data written to the region with a different shadow mask bit value would reset the shadow mask bit to the first state];

detecting a second write operation to the second region of local memory [All write operations are detected by the memory management unit (Paragraph 11)];

detecting that the second shadow mask bit is in the first state [Memory management unit must check state of WO bits, to decide where to translate the data];

cloning the second write operation to the second region of local memory; operation [When WO is 11, write operation is cloned to both memories (Paragraph 90)]; and

writing the cloned second write operation to system memory (Paragraph 18).and

11. As per claim 8, Durrant discloses that in a graphics processing system, including a graphics processing unit, a local memory associated with the graphics processing unit, a co-processor and a system memory, a method for memory management, the method comprising [A graphics processing system is a type of multiprocessor system (Paragraph 18):

initiating an operation to write vertex data in the local memory [vertex data is a type of data (Paragraph 11)];

detecting that the region of local memory to which the vertex data is to be written is a region to be shadowed [(Durrant describes data can be one of four states (Paragraph 15, Paragraphs 86-90)];

cloning the vertex data to be written to local memory [When WO is 11, write operation is cloned to both memories (Paragraph 90)];

routing the cloned vertex data to system memory [Translated address would route the cloned vertex data to system memory].

12. As per claim 9, Durrant discloses the method of claim 8 wherein said detecting comprises determining a shadow mask bit associated with the region of local memory to be in a state indicative of requiring a shadow operation [Since each WO bit is assigned to write data, the WO bit is associated with a region of the local memory the data is written into (Paragraph 86-90)].

13. As per claim 10, Durrant discloses the method of claim 9 wherein said routing includes,

translating an address of the region in local memory into an address in system memory (Paragraph 15); and

writing the vertex data to the system memory at the address provided by the translating operation (Paragraph 15).

14. As per claim 11, Durrant discloses the method of claim 8 wherein said routing includes,

translating an address of the region in local memory into an address in system memory (Paragraph 15); and

writing the vertex data to the system memory at the address provided by the translating operation (Paragraph 15).

12. As per claim 12, Durrant discloses a memory system comprising:

a central processing unit (Fig 11, Ref 56);

a second processor (Fig 11, Ref 62);

a local memory associated with said second processor (Fig 11, Ref 66);

a shadow unit coupled to said central processing unit and including a shadow bit mask having a plurality of bits, each bit associated with a region of the local memory (Fig 11, Ref 28); and

an address translator coupled to said shadow unit (Fig 11, Ref 28).

15. As per claim 13, the system of claim 12 wherein said address translator includes a translation cache having a pool of translations (Fig 7, Ref 270).

16. As per claim 14, Durrant discloses a graphics processing system comprising:

a central processing unit (Fig 11, Ref 56);

a graphics processing unit (Fig 11, Ref 62);

a graphics processing unit frame buffer [obvious in a graphics processing system];

a coprocessor unit [obvious in a graphics processing system];

a coprocessing unit frame buffer [obvious in a graphics processing system]; and

a shadow unit coupled to said central processing unit and coprocessing unit frame buffer, said shadow unit including a shadow mask adapted to track regions in said graphics processing unit frame buffer to be shadowed in the coprocessing unit frame buffer [Each entry in the memory has a WO bit which discloses shadowing, thus each entry is a region of the memory tracking shadowing (Fig 11, Ref 28)].

## *Conclusion*

17. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 31, 2005

Leonid Kravets
Patent Examiner
Art Unit 2189

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER